A Quick Fix for Poor Capacitor, Inductor and DC/DC Impedance Measurements

Shaking Bugs Out of SPI Buses

Five Tips for Improving ESD Protection
In the first post of this series, we considered some of the challenges of debugging embedded systems in general and I2C buses in particular. Modern digital oscilloscopes equipped with powerful trigger/decode software for the serial protocol in play go a long way toward easing the path to a properly functioning embedded system. Now we’ll consider the particularities of the Serial Peripheral Interface and how the proper tools can make debugging SPI buses easier.
The Serial Peripheral Interface, which was developed by Motorola, is a master/slave synchronous communication system with data rates up to 50 Mb/s and typical data packet sizes of 8 to 16 bits. SPI uses four signals and four data-transfer formats. The four signals are clock (SCK), Slave Select (SS); Master Output, Slave Input (MOSI), and Master Input, Slave Output (MISO). The four formats depend on the condition of the clock polarity (SPOL) and clock phase during data transfer. The data-transfer format is set on each master or slave and the master/slave combination must have a matched data-transfer format to establish a link.

As with I2C trigger/decode software, today’s SPI trigger/decode software is well tailored to the debugging requirements of designers and technicians. Referring to the bottom left of Figure 1 within the SPI dialog box, one may trigger on standard 3-wire SPI signals or use the preset Serial I/O Port (SIO) or Simplified SPI (SSPI) settings.

In the Format field of the Trigger dialog box, timing-diagram buttons provide a choice between Clock Phase (CPHA) and Clock Polarity (CPOL) to customize triggering for specific applications. In the interest of simplicity, these formats are automatically selected when you choose between the SIO and SSPI settings.

As with the I2C trigger/decode software, the SPI version enables you to trigger on specific data values in either binary or hex formats. Binary triggering lends the flexibility of triggering on individual bits in a pattern while hex triggering simplifies the setup of long data pattern triggers.

In the next issue of Modern Test & Measure, we’ll look at debugging embedded-system buses in the UART format.

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Using **Wi-Fi** to **Count the Number of People** in a Room

A team of researchers in UC Santa Barbara professor Yasamin Mostofi’s lab have proven that Wi-Fi signals can be used for more than just providing Internet access, they can actually be used to count the total number of people in a given space.

“Our approach can estimate the number of people walking in an area, based on only the received power measurements of a Wi-Fi link,” said Mostofi, a professor of electrical and computer engineering.
He explained that his group’s solution did not require people carry around Wi-Fi-enabled devices for them to be counted. Rather, to achieve this people-counting feat, the team placed two Wi-Fi cards at opposite ends of a target area (approximately 70 square meters) and by using only the received power measurements of the link between the two cards, they were able to estimate the number of people walking in that area.

So far, tests have been conducted with up to and including nine people in both indoor and outdoor settings.

“This is about counting walking people, which is very challenging,” said Mostofi. “Counting this many people in such a small area with only Wi-Fi power measurements of one link is a hard problem, and the main motivation for this work.”

This method of counting relies largely on the changes of the received wireless signal. You see, people being in a given space weakens the signal as it hampers the direct line of sight between the Wi-Fi cards; human bodies cause the signal to instead scatter, which results in something called multi-path fading. The team was able to develop a mathematical framework based on these two phenomena, and in turn propose a solution for estimating the number of people walking in the space itself.

Beyond the obvious impressiveness of having discovered a new use for something so ubiquitous, this technology could serve several different purposes. Most notably, it could be used estimate the number of people in a space within a home or office building so air conditioning and heating systems can be adjusted according to the level of occupancy.

“Stores can benefit from counting the number of shoppers for better business planning,” Mostofi added.

Additionally, search-and-rescue operations could benefit from this technology, as it would allow emergency response personnel to detect how many people are in a particularly difficult-to-reach space.

The group’s findings are scheduled for publication in the Institute of Electrical and Electronics Engineers Journal on selected areas in Communications’ special issue on location-awareness for radios and networks.

You can read more about the research the group is working on via their project page.
HARDWARE DESIGN MADE EASY.

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Electro static discharge (ESD) poses a real threat to product quality, and is difficult to spot. ESD standards are continuously updated to keep pace with changes in technology and new test equipment formats. Trends like the increased sensitivity of electrical components, or the implementation of PXI or AXIe test systems, can present new ESD challenges. While the flexibility and configurability of PXI and AXIe test equipment provides a lot of advantages, it opens the door to more ESD risks than enclosed benchtop instruments.
ESD challenges and implementing best practices will reduce ESD failures and protect your investment in electronic devices and modular test equipment. A fresh look at your production areas may produce some surprising static generators that require immediate removal.

This article offers a few tips to keep your electronics functioning properly and your test areas free from sources of ESD. Sensitivity to ESD varies by device. Here, we will look at a wide range—from benchtop, PXI and AXIe test instrumentation to fabrication of high frequency Indium Phosphide (InP) and Gallium Arsenide (GaAs) devices, which are typically more sensitive to ESD.

Visible only through high power magnification, it is clear that ESD damage caused this failure. Poor ESD practices have the ability to not only damage your test equipment, but also the electronic devices you are testing.

The ESD standard, ANSI/ESD S20.20 2014 includes modifications to help manufacturers better protect their devices from this type of ESD damage. The earlier 2007 version of the standard focused on electrostatic discharge from the Human Body Model (HBM) greater than or equal to 100 volts. The HBM simulates a human discharging through a device to ground. The updated standard added a focus on discharge from the Charged Device Model (CDM). The CDM simulates the discharge of a charged device when it comes in contact with a conductive material. One example of a CDM is an electronic device that was charged in transit and then discharged when placed in a metal test fixture. The machine model (MM) represents a discharge from an object to the component. The object could be a metallic tool, production equipment, or even test equipment coax cable. The new standard provides ways to plan your test area to prevent ESD damage from humans, devices under test and production test equipment.

**Tip 1.** Safe handling of ESD sensitive instruments starts with a good procedure and training

Prevention of ESD damage to your PXI test system and DUTs starts with proper handling of the modules. If your test line personnel are familiar with traditional enclosed test equipment handling, your production line is off to good start. Personnel may be trained on the safe ESD handling of DUTs. This includes heeding any front panel warnings of the traditional enclosed test equipment. Traditional test equipment can be moved or handled without ESD controls since the equipment is enclosed, sealed and tested for ESD. The outer cover is a Faraday cage protecting the internal circuitry. With PXI or AXIe modular test equipment, more care needs to be taken. Reconfiguring modular test equipment requires ESD protection. Behind the modular front panel, ESD sensitive circuitry and possibly high performance connections may be exposed. Keysight’s M9370A PXIe Vector Network Analyzer (Figure 2) displays the ESD symbol on the side panel, a clear indication that inserting or removing the module should be done with ESD protection such as a ground strap.

**Tip 2.** Periodically check ESD static bags

Everyone knows the pink ESD static bags are safe, right? We recently found out that this is not always the case. Legitimate ESD bags have a finite life and need to be occasionally sample checked to make sure they are not able to generate static. Also, some pink ESD bags are not authentic. Though they are colored pink, unscrupulous suppliers are selling low priced bags that are not ESD safe. Checking your ESD packaging suppliers regularly is also a good ESD practice.

**Figure 1.** Magnified views of a FET-based switch with ESD damaged gate (circled in red).

**Figure 2.** Keysight’s M9371A PXIe Vector Network Analyzer with ESD symbol circled in red.
Tip 3. Proper use of canned air dusters

Technicians often use canned pressurized air dusters to spray PCAs for cleaning or cooling. We watched a troubleshooting process where technicians were using the canned air duster to troubleshoot a circuit. We used our static field meter to measure the static build up from the spraying process. When the can was help upright, the duster can sprayed mostly air and there appeared to be minimal to no static build up. However, when the can was turned upside down, a liquid propellant sprayed, which generated 1500 volts, as measured with a charge plate. The liquid propellant created enough friction to generate a significant level of ESD.

Tip 4. Periodically check PXIe plastic slot blockers

Another ESD issue was identified in the PXIe test instrument production area. During testing of a PXIe 18-slot chassis, slot blockers were used to fill empty slots in the chassis. Slot blockers are plastic baffles inserted into empty slots to provide the proper air flow for cooling the instrument. We were concerned that these plastic slot blockers could generate a charge right next to sensitive PCA components on the nearby card. We tested the slot blockers from Keysight and a non-Keysight PXIe test equipment supplier to see if they would generate charge while being handled. We found that the non-Keysight supplier’s slot blockers generated charge up to 10,000 volts per inch. Having a plastic part charged this high poses an ESD risk for the nearby components. The Keysight slot blockers did not charge more than 100 volts/inch when handled. Parts that are presumed to be ESD safe should be periodically checked.

Tip 5. Periodically test the workstation ground path

ESD damage can directly hurt your bottom line. As part of our vendor quality audits, we often review our suppliers’ ESD procedures. On one of these visits, a supplier was having issues making their yield goals for an electronic component. This supplier had a good, updated ESD procedure that the production team followed in their day to day activities. However, they suspected that some of their line failures could be ESD damage. As part of our audit, we asked them to check the workstation ground path. In this case, we found some production stations had been moved but the static ground had not been reconnected. The workstations were not at zero volts and it was possible to damage the sensitive electronic components when they were placed on these workstations. Poor workstation grounding and the poor ESD protection it caused was found to be a factor in the mysterious yield issues they were having. In this case, the ESD damage directly was causing reduced process yields and wasted dollars.

PXIe modular test system use is growing rapidly. The more open design makes ESD protection even more important. Revisiting your ESD practices for your PXIe test area is a good idea. Make an assessment of how well your test area is preventing ESD damage and look for static generators lurking in your test area. ESD damage is hard to spot but can create real failures. Good ESD practice will reduce test area down time and help prevent ESD failures on the devices your team is testing.

Poor workstation grounding and the poor ESD protection it caused was found to be a factor in the mysterious yield issues they were having.
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A Quick Fix for Poor Capacitor, Inductor and DC/DC Impedance Measurements

By Steve Sandler – Picotest

Designing or optimizing a Voltage Regulation Module (VRM) requires output impedance data from the VRM, as well as impedance data for the filter inductors and capacitors to support the simulation models. Vendor data is often incomplete, erroneous, or difficult to decipher in terms of the setup involved to make the measurement and therefore, we often need to collect this data ourselves.
The measurements need to be performed over the entire frequency range of interest, typically in the low kHz to 1 GHz region, depending on the application. Because of this very wide frequency range we generally turn to S-parameter-based measurements. High performance simulators, like Keysight’s ADS can directly incorporate the S parameter component measurements in AC, DC, transient and harmonic balance simulations while including the finite element PCB models.

While extremely useful, standard S-parameter measurements frequently aren’t sufficient. What’s really needed is an extended range, partial S2p measurement. In this article, I’ll explain why you need it and how to make this improved measurement.

**S-parameter Impedance Basics: How they work**

S-parameters are a simple method of performing measurements over a very wide frequency range. The measurement is performed using a fixed resistance port rather than a high impedance probe. Two options are available for measuring impedance with S-parameters: the first option is a reflection measurement and the second option is THRU measurement.

**One Port or Two? Why Partial?**

The reflection, or 1-port, measurement is the simplest, since it only requires one cable. However, it also requires a more complex calibration, generally consisting of an OPEN calibration, a SHORT calibration and a LOAD or MATCH calibration of the port used for the measurement. Most Vector Network Analyzers (VNAs) include the transformation from the S-parameter reflection measurement (S11 or S22) to impedance, but it’s quite simple. Using port 1 as an example, the reflection for a given reference impedance, $Z_{ref}$ (typically 50Ω) the relationship between $S_{11}$ and the device impedance is shown in Table 1.

**Table 1. 1-Port Transformations**

<table>
<thead>
<tr>
<th>1-Port Reflection Measurement</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_{11}(Z) = \frac{Z - Z_{ref}}{Z + Z_{ref}}$</td>
</tr>
<tr>
<td>$Z(S_{11}) = Z_{ref} \cdot \frac{1 + S_{11}}{1 - S_{11}}$</td>
</tr>
</tbody>
</table>

The 2-port measurement can be performed by placing the device to be measured either in series or in shunt with the measurement ports. The relationship between $S_{21}$ and the device impedance is shown, for both the series and shunt configuration in Table 2.

**Table 2. 2-Port Transformations**

<table>
<thead>
<tr>
<th>2-Port Series Measurement</th>
<th>2-Port Shunt Measurement</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_{21}<em>{\text{Series}}(Z) = \frac{2 \cdot Z - Z</em>{ref}}{Z + 2 \cdot Z_{ref}}$</td>
<td>$S_{21}<em>{\text{Shunt}}(Z) = \frac{2 \cdot Z}{Z + 2 \cdot Z</em>{ref}}$</td>
</tr>
<tr>
<td>$Z(S_{21_\text{series}}) = \frac{2 \cdot Z_{ref}}{S_{21_\text{series}}} - 2 \cdot Z_{ref}$</td>
<td>$Z(S_{21_\text{shunt}}) = \frac{2 \cdot Z_{ref}}{1 - S_{21_\text{shunt}}}$</td>
</tr>
</tbody>
</table>

**DC Ground Loop**

An additional issue arises for the 2-port shunt-thru measurement due to a DC ground loop which occurs as a result of the RF ground at the VNA and the series resistance of the interconnecting measurement cables. The Keysight E5061B VNA has a semi-floating input on the low frequency gain-phase ports, eliminating this DC ground loop for low impedance measurements up to 30 MHz. For the E5061B high frequency ports and other VNAs in general, the DC ground loop must be minimized using a common mode coaxial transformer, such as the Picotest J2102A, otherwise, the low frequency measurements will be inaccurate.

The setup diagrams for these impedance measurement options are shown in Figure 1.
The simulations in Figure 2 show the S-parameter magnitude, for each measurement technique, as a function for the device impedance. The measurements all lose sensitivity as the S-parameter magnitude approaches 1.0.

Figure 1. Basic Schematics for the 1-port and 2-port impedance measurements.

Figure 2. S-parameter magnitude as a function of the device impedance.
A higher resolution view of the S-parameter magnitude from 0.95 to 1.0 is shown in Figure 3.

Setting the measurable S-parameter (either S11, S22 or S21) to a minimum of 40E-6 to allow a reasonable signal to noise margin and a maximum of 0.95, the ranges for each measurement are shown in Table 3.

Table 3. Measurement Impedance ranges

<table>
<thead>
<tr>
<th>Measurement</th>
<th>Min</th>
<th>Max</th>
<th>Realistic measurement Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-port Series</td>
<td>1.3kΩ</td>
<td>2kΩ</td>
<td>0.5Ω-2.5kΩ</td>
</tr>
<tr>
<td>2-port Series</td>
<td>5.3Ω</td>
<td>2.5MΩ</td>
<td>50-2.5MΩ</td>
</tr>
<tr>
<td>2-Port Shunt</td>
<td>1mΩ</td>
<td>475Ω</td>
<td>0.5mΩ-200Ω</td>
</tr>
</tbody>
</table>

**What Range Do We Need?**

Since we are typically measuring VRMs, PDN’s, capacitors and inductors, the minimum impedance measurement is in the range of milliOhms, whether it is inductor DCR, VRM output impedance or capacitor ESR. This requires the 2-port shunt measurement.

The measured S-parameter file must be valid for the complete simulation frequency range. Establishing the measurement range to be from 1 kHz to 500 MHz and using the realistic measurement range, we can determine the maximum inductance or capacitance that can be measured using the 2-port shunt measurement.

\[
C_{min} = \frac{2}{2\pi \cdot 1kHz \cdot 200\Omega} = 0.8uF
\]

\[
L_{max} = \frac{200\Omega}{2\pi \cdot 500MHz} = 64nH
\]

Using the 2-port shunt measurement, the minimum capacitance that can be measured is 800 nF, precluding the measurement of high frequency decoupling capacitors. The maximum inductance that can be measured is only 60 nH. Even if the inductor is assumed to be resonant frequency far below 500 MHz, the maximum inductance that can be measured is far less than 1 uH, precluding the measurement of ferrite beads and most filter inductors.

Another issue that arises in making the full 2-port shunt measurement is that S21, S11 and S22 are all measuring the same device and therefore the same impedance range. As already explained above, these measurements fall below the range of the 1-port measurement. For example, while measuring an inductor, the DCR will be measured as S11 and S22 and while measuring a capacitor the ESR will be measured using S11 and S22, since these 1-port terms will be invalid at low impedance levels. Hence the reason for a “partial” 2-port thru measurement. We will only keep the S21 term and remove the S11 and S22 terms as they are invalid at impedance levels below 0.5Ω. Some instruments allow saving the measurement as a Touchstone impedance file, which is a partial 2-port S-parameter file.
Extending the 2-Port Range

The measurement can be scaled using series resistors, effectively increasing the port reference impedance and allowing the measurement of decoupling capacitors and larger inductors. A schematic of this measurement is shown in figure 4.

For example, adding a 450Ω series resistor modifies the reference impedance to be 500Ω, shifting the measurement range up by a factor of 10. In some cases, the added series resistors can be accommodated by using an attenuating transmission line scope probe. Scaling factors of 1, 5, 10 and 20 are commercially available as 1-port probes. A pair of probes can be used to make a 2-port extended range measurement. The measurement range for various values of series resistors are shown in table 4.

Table 4. Measurement Impedance ranges for various series resistor values

<table>
<thead>
<tr>
<th>Series Resistor</th>
<th>Min</th>
<th>Max</th>
<th>Realistic measurement Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>0Ω (1:1)</td>
<td>1mΩ</td>
<td>475Ω</td>
<td>0.5mΩ-200Ω</td>
</tr>
<tr>
<td>200Ω (5:1)</td>
<td>5mΩ</td>
<td>2.4kΩ</td>
<td>5mΩ-1kΩ</td>
</tr>
<tr>
<td>450Ω (10:1)</td>
<td>10mΩ</td>
<td>4.75kΩ</td>
<td>10mΩ-2kΩ</td>
</tr>
<tr>
<td>950Ω (20:1)</td>
<td>20mΩ</td>
<td>9.5kΩ</td>
<td>50mΩ-4kΩ</td>
</tr>
</tbody>
</table>

Figure 4. Adding series resistors to extend the impedance range of the 2-port shunt measurement.

The impedance transformation with the series resistors included is shown in Table 5.

Table 5. Impedance transformation including series resistors

\[
S21(Z) = \frac{2Z}{RS + 2Z + Z_{ref}}
\]

\[
Z(S21) = \frac{Z_{ref} + RS}{2} \cdot \frac{S21}{1 - S21}
\]

For measurements at either extreme of the measurement range, be sure to perform a full fixture removal calibration or full 1-port calibration on both parts as well as a THRU calibration. If series resistors are included, perform the THRU calibration with the series resistors included in the setup.

Figure 5. Measurement of a 0.1 uF capacitor with RS=200Ω shows the resonance resulting from the capacitor ESL and the SMA connector capacitance of approximately 1 pF.
The SOL calibration is performed at the cable and the additional capacitance from the series resistor connectors resonates at approximately 850MHz degrading the accuracy of the measurement.

Including the series resistors on the circuit board with the capacitor removes the additional capacitance and greatly improving the high frequency accuracy as seen in Figure 6.

Conclusion

Implementing the extended range technique and saving only the S21 data or a Touchstone Z data file offers a method of scaling the measurement to optimize the measurement window. Added benefits to note are the extension resistors reduce the loading when measuring lower power VRM’s. This technique can also be used for measuring the output impedance of voltage references and closed loop opamps and is supported by the Picotest non-invasive stability measurement as well.

References

How to Design for Power Integrity (video): https://youtu.be/ejAApIv1cR8?list=PLtq84kH8z9HIYqBYDsP7TboBpfKdzl8

Selecting a VRM (video): https://youtu.be/0J6g9H_m4?list=PLtq84kH8z9HIYqBYDsP7TboBpfKdzl8