LATCHED COMPARATOR
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CIRCUIT SCHEMATIC OF LATCHED COMPARATOR:

[Diagram of a latched comparator circuit]
CIRCUIT SCHEMATIC OF NON OVERLAPPING CLOCK GENERATOR:

WAVEFORMS OF NON OVERLAPPING CLOCK GENERATOR:

LTSPICE – NONOVERLAPPING CLOCK
WAVEFORMS OF LATCHED COMPARATOR:

LTSPICE – LATCHED COMPARATOR

LTSPICE – COMPARATOR (ALONE)
WORKING:

The clock signals 1 and 2 are generated from the non overlapping clock generator. Clock 2 is fed to the Latched comparator while the clock 1 is fed to the D flip flop.

When V+ is high and V- is low, only M9 and M10 (top right) conduct. The drain of M6 is then charged to VDD. This turns off M8. M7 is already off because of the high V+ signal. When clock 2 is high, all the lower NMOS conduct; R and S are short to ground. When clock 2 goes low, the voltage VDD is short to S. Thus when V+ > V-, the latch is Set. The vice versa is also true.

In order to remove the glitches in the R and S waveforms, we further pass them to RS flip flop. The values are held using the D flip flop.

REFERENCE:

- Understanding Delta-Sigma Data Converters by Richard Schreier and Gabor.C.Temes