INTERNERSHIP SUMMER 2011

PROJECT REPORT

Power Factor Correction for 1500W SMPS

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The following report embodies the accomplishments during the internship at KB Electronics, Mumbai, India during the period June-July, 2011.

During the initial two weeks, I was involved in soldering leaded as well as Surface Mount Devices (SMD) components on PCB for different products like battery chargers, SMPS, etc. It involved studying the circuit diagram along with the assembly layout, co-relate the two and then solder the components accordingly. Soldering SMDs was a new experience for me. It involves careful and intricate soldering, so as not to short the adjacent two terminals of ICs due to excess solder. Soldering of resistors and capacitors was comparatively easier.

Later, I was involved in development of the software algorithm for MPPT solar charger. The MPPT Algorithms that I had presented in the Graduate Research Seminar in the last semester did help me a lot in this regard. We chose a Hill climbing and Perturb and Observe, 3-point algorithm, to take into account the irradiance changes that might affect the correct tracking of the I-V curve of the PV panel. I also got to work with actual solar panels, observing the changes in the short circuit current through the panel due to shadow effects. However, this project has taken a back seat due to lack of consistent sunlight in the monsoon season. Currently I am working on the Power factor correction circuit for a 1500W SMPS.

Power factor correction involves improving the power factor (cosine of the phase angle between RMS input voltage and RMS current of the mains) of the circuit to unity. The input capacitor filter has a typical PF ≈ 0.63. This implies that the circuit extracts more current from the mains than necessary. The additional RMS current does not perform any useful work and is wasted as energy in the harmonics and dissipated as heat in the circuit. This decreases the efficiency of the overall circuit considerably. Hence, we apply PFC to improve the efficiency as well as reduce the energy content of the harmonics. The PFC stage includes a boost convertor since its input current, is the same as the inductor current, continuous in nature. This makes it easy for PFC. The only disadvantage is that the output voltage becomes high, in this case the 410VDC bus. Due to the inherent nature of the boost circuit is it not short circuit protected, since the switching device is in parallel with the input source. To reduce the stress on the inductor, L1 and the freewheeling diode, D1 due to a short-circuit condition as well as when the output voltage falls below the input voltage (an anomalous condition for a boost convertor), a diode, D2 is connected in parallel with the inductor as well as the freewheeling diode. This diode is reverse biased when the boost converter is functioning properly. The circuit diagram of the entire circuit is attached separately.

I read the literature on PFC that the company gave me along with datasheets and application notes relating to the same. We are using Unitrode UC3854 IC as the heart of the PFC stage. This PFC stage feeds the DC-DC converter stage of a 48V 32A SMPS. The PFC stage will create a 410
VDC bus for the DC-DC converter. The input range is 170-270 VAC, with expected efficiency of 95% (as told to be considered by my senior).

The reason for selecting UC3854 is that it has a unique feature that combines a squarer, multiplier and divider circuit into a single block. This block multiplies a fraction of the output voltage, obtained through a voltage divider, with the input AC current and then divides it by the square of the input voltage. This keeps the gain of the voltage-feedback loop constant, increasing the stability of the system. 'Cusp distortion', a phenomenon that occurs at the beginning of the rectified sine wave, is also reduced. An internally generated 7.5V reference is available. UC 3854 also has internal over-voltage protection and current limiting and a soft-start feature. Consider a situation where due to some fault, the DC-DC converter starts before the DC bus capacitor bank comprising of C1, C2, C3 and C4 is fully charged. The inrush-limiting resistor, RT1 is shunted, before the DC-DC convertor starts and hence will not play any part in limiting the current. There will be a huge inrush of current to fully charge the capacitor bank without any limiting device, bringing the MOV1 into conduction or blowing the fuse, F1. To avoid this soft-start feature is necessary.

Designing of the PFC stage has been accomplished by referring the application note for UC 3854. The application note had the necessary steps needed to design the peripheral circuitry for the optimum working of 3854. The necessary calculations are performed and have been attached as a scanned document separately. However, it is expected that some of the calculations will need further fine-tuning during actual testing, after cascading this circuit with the DC-DC convertor stage. All the resistors are of ¼ W unless specified otherwise. Some of the resistors and capacitors will be SMDs and some will be leaded. The resistor and the capacitor for setting the frequency of the internal oscillator of 3854, Rset and CT will be leaded. The current sense resistor, Rsense, connected on the return power rail, is a 2W resistor. The high value resistors like RVi, Rvd, RVf, Rvf2, RVac and RB1 will be split into smaller value resistors to be connected in a chain-like manner in series, so that they all can have a lower power rating of about ¼ W.

In addition to the PFC stage, the boost stage and the EMI/RFI noise rejection stage are also designed.

I observed the waveforms of the typical capacitor input filter, on an oscilloscope. It leads to an inrush current, which can be in the range of 10-100s Amperes depending on the input supply range and the current limiting technique used. A very high current pulse occurs at the peak of the input sine wave, when the capacitor charges for the very first time. This pulse needs to be limited so that the rectifier diodes are not damaged, though the diodes are rated to withstand a high current for a maximum period of 8-10ms. The parasitic resistance of the input filter components is the only resistance available to the inrush current if no further protection
scheme is used. A metal oxide variistor MOV1 is used to supplement the inrush current limiting. It bypasses the current to the ground once its rating has exceeded, protecting the further circuitry. Similarly, a fuse, F1 is used for the same purpose. Care is taken to ensure that the fuse rating is lower than the switcher rating, so that the fuse blows first in case of an over-voltage protecting the switcher. Typically, a thermistor (NTC characteristics) or a resistor paralleled with a SCR used as an additional protection. We have used a 1Ω resistor, RT1 shunted with a relay, to prevent excessive power dissipation in this resistor once the circuit is operating in the normal conditions. The inrush relay shorts the resistor when the voltage reaches 300 VDC and normally opens at 270 VDC. DC-DC converter starts when the voltage level reaches 390 VDC and shuts down at 360 VDC. These levels are chosen arbitrarily taking into account hysteresis and transients. There are many additional factors to consider when designing the circuit practically, which is not the case in theory.

The EMI/RFI input filter designing was the next stage. There are two types of noise that can interfere with the circuit – Common mode noise (noise developed between the earth and each of the two power rails) and differential mode noise (noise developed between the two power rails with respect to the earth). The noise is caused because of the fast rise and fall times of the switching devices, diodes, etc. If it is not filtered properly, it might lead to ‘ground voltage bumps’. This can lead to ground referencing problems in power supplies that use a common ground/return line. The basic EMI/RFI filter has an L-C filter, consisting of X capacitors, C1, C2 and C3 and Y capacitors C4, C5, C6, C7. The X capacitors are so called because they are connected 'across' the power rails, and the Y capacitors are for the common mode noise rejection. The inductors are connected in a 'common mode configuration' such that they are in anti-phase to the differential mode noise and it is cancelled out. These interferences can be further reduced by careful layout design.

Designing of the inductor of the PFC boost stage and the transformer, for common mode noise rejection in the EMI filter section, required extensive reading and help from seniors in the company. For the EMI transformers, T1 and T2, the core was selected first and then depending on the number of turns required to satisfy the ampere-turns ratio, inductance was calculated accordingly. Datasheet of Cosmo Ferrites was referred for this purpose. We have incorporated a two-stage EMI input filter for better noise rejection.

The inductor, L1 of the boost stage is operating in the continuous conduction mode. Hence, the average DC current (magnetizing force, H) through it is high though the ripple content is comparatively lower. The core might saturate due to this DC current. This makes the design 'saturation limited'. Therefore, it is necessary to use a gap in the core to avoid saturation. Due to gapping, the core can support high magnetizing force, without saturating, since most of the energy is present in this gap. It also increases the working limits of the flux density, B and the residual/remnant flux level reduces. This is caused by a tilt in the hysteresis curve, indicating a
reduction in the permittivity of the core as well as inductance, which can be compensated by increasing the number of turns, if necessary. The normal working, current density for fan cooled power supplies is considered to be about 400 c.m/A (Circular mils/Ampere), which corresponds to 5A/mm$^2$. One circular mil is the area of a circle 0.001 inch in diameter. To reduce the space on the PCB we have considered a density of 250c.m/A or 8A/mm$^2$. This might have cause heating of the core. However, the temperature rise was within limits, which was verified by experiments. Next was to consider the 'skin effect' (tendency of current to flow close to the surface of the conductor at higher frequencies), to select the wire gauge properly and hence save some winding area in the core. Some compromises are made to save the cost, layout space and still achieve optimum efficiency of the design.

All the necessary calculations and assumptions have been shown in the scanned document.

The ratings of the switching MOSFETs, Q$_1$ and Q$_2$, were selected keeping into mind that they are able to handle the current capabilities at the lower end of the voltage range. I observed the waveforms of the actual switching that takes place at the switching frequency, 70 KHz in this case, with respect to the line frequency. The dynamic change in the duty cycle/pulse width occurs for about 700 times per half sine wave, for 70 KHz switching frequency. I have tried to represent this phenomenon in the Figure-1. The sine wave shown is the one after being rectified by the bridge circuit, having a frequency of 120Hz. The maximum pulse width occurs at the beginning of the input waveform when the voltage is the minimum, close to zero, and then gradually decreases as the voltage increases.
I have learnt a great deal in these two months and still have five months to wrap up. I will strive to be a good designer at the end of this internship stint. During the next five months, I might work of some of their other products like battery chargers. I might also do some testing of their products, before they are dispatched to the customers. Resuming work on the Buck converter for MPPT solar charger will be done as and when instructed by my seniors, probably by September 2011.

REFERENCES

1. *Unitrode UC 3854 Datasheet and Application Note*
2. 'Switch mode Power Supply Handbook' By Keith Billings
3. 'High-frequency Switching Power Supplies: Theory and Design' By George Chryssis

References 2, 3 are for designing parts of the circuit other than the PFC stage as well as for general reading.